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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,985	07/07/2003	Hajime Akiyama	239861US0	6382
22850	7590	02/01/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			NADAV, ORI	
1940 DUKE STREET			ART UNIT	
ALEXANDRIA, VA 22314			PAPER NUMBER	
			2811	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/612,985

Applicant(s)

AKIYAMA ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-15 is/are pending in the application.  
4a) Of the above claim(s) 8-15 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4, 6 and 7 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Election/Restrictions***

Rejoinder of withdrawn process claims will be granted when the device claims are found allowable, and the withdrawn process claims include all the limitations of the allowable device claim.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support for a second auxiliary dielectric layer disposed between said first auxiliary dielectric layer and said primary dielectric layer, wherein the first auxiliary dielectric layer is junctioned to said primary dielectric layer, as recited in claim 3.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (5,476,809) in view of Akio (Jp9-172189).

Kobayashi teaches in figure 6 and related text a dielectric separation type semiconductor device, comprising:

A semiconductor substrate 4;

a primary dielectric layer 3 (the upper extended horizontal layer 3) disposed adjacent to a whole region of a first main surface of said semiconductor substrate;

a first conductivity type first semiconductor layer 17 of a low impurity concentration disposed on a surface of said primary dielectric layer 3 in opposition to said semiconductor substrate 4 so that said primary dielectric layer is sandwiched between said first conductivity type first semiconductor layer 17 and said semiconductor substrate;

a first conductivity type second semiconductor layer 25 of a high impurity concentration formed selectively on the surface of said first semiconductor layer;

a ring-like insulation film 3 (the sloped layer 3 which extends from the top surface of the semiconductor layer 17 to the substrate 4) disposed so as to surround an outer peripheral edge of said third semiconductor layer;

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a first main electrode 21 disposed in contact with a surface of said second semiconductor layer;

a sheet-like back-surface electrode 15 disposed adjacent to a second main surface of said semiconductor substrate on a side opposite to said first main surface of said semiconductor substrate; and

a first auxiliary dielectric layer 3 (the horizontal part (or the bottom part) of sloped layer 3 which extends from the top surface of the semiconductor layer 17 to the substrate 4. Said horizontal part is located below layer 3) disposed below said second semiconductor layer 25

wherein a second auxiliary dielectric layer 3 (the lower extended horizontal layer 3) is disposed between said first auxiliary dielectric layer and said primary dielectric layer, and wherein said second auxiliary dielectric layer is junctioned to the semiconductor substrate and the first auxiliary dielectric layer 3.

Kobayashi does not teach a second conductivity type third semiconductor layer of a high impurity concentration disposed so as to surround an outer peripheral edge of said first semiconductor layer with a distance, wherein a second main electrode disposed in contact with a surface of said third semiconductor layer.

Akio teaches in figure 2 and related text a second conductivity type third semiconductor layer 19, 20 of a high impurity concentration disposed so as to surround an outer peripheral edge of said first semiconductor layer with a distance, wherein a second main electrode disposed in contact with a surface of said third semiconductor layer, and

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a ring-like insulation film 14 disposed so as to surround an outer peripheral edge of said third semiconductor layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a second conductivity type third semiconductor layer of a high impurity concentration disposed so as to surround an outer peripheral edge of said first semiconductor layer with a distance, wherein a second main electrode disposed in contact with a surface of said third semiconductor layer in Kobayashi's device in order to provide better electrical isolation to the device by a well known guard ring technique.

Regarding claim 2, Kobayashi teaches a first auxiliary dielectric layer is so disposed that one end thereof is located at a position corresponding to said first main electrode and extends over a region of a size not smaller than 40% of a distance between said first main electrode and said second main electrode.

Regarding claim 3, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first auxiliary dielectric layer shaped in a cylindrical form in Kobayashi's device in order to simplify the processing steps of making the device.

Regarding claim 4, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first auxiliary dielectric layer shaped in a bowl-like form in Kobayashi's device in order to provide better insulation between the active areas of the device.

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Regarding claim 6, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second auxiliary nitride dielectric layer in Kobayashi's device in order to provide better insulation between the active areas of the device.

Regarding the process limitations recited in claim 6 ("second auxiliary dielectric layer is formed by a thermally nitrided film or alternatively by a CVD nitride film") these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 7, Kobayashi teaches a semiconductor substrate includes a p-type semiconductor region formed integrally with said semiconductor substrate.

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***R s p o n s   t o   A r g u m   n t s***

Applicant's arguments with respect to claims 1-4 and 6-7 have been considered but are moot in view of the new ground(s) of rejection.

***C o n c l u s i o n***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should b   faxed to TC 2800 via th   TC**



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**2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized flourish at the end.

O.N.  
1/26/05

ORI NADAV  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800